REMARKS

Applicant acknowledges with appreciation the allowance of claims 1-5 and 8-13. Claims 21 and 22 have been properly renumbered as claims 20 and 21, respectively. Claims 18-20 have been amended. New claims 22-23 have been added. Claims 1-5, 8-13 and 18-23 are pending. Applicant reserves the right to pursue the original and other claims in this and in other applications.

Claims 18-22 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Reconsideration is respectfully requested.

Claim 18 has been amended to include the limitation that source regions or drain regions are "*surrounded* by element separation films on a support substrate, the element separation films being oxide films." Therefore, claim 18 should be allowable.

Claim 19 has been amended to delete the limitation "coupled to the gate electrode through another element." Therefore, claim 19 should be allowable.

Claim 22, renumbered as claim 21, depends from claim 18 and further recites a field cell comprising a heat conduction part. The Office Action contends that how the field cell has a heat conduction part is not clear. Applicant respectfully disagrees. The field cell 57 having a heat conduction part 55 is shown in FIGS. 7A-7B. *See* Specification on page 29, lines 3 to 17. Therefore, renumbered claim 21 should be allowable.

Claims 18-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,919,235 ("Yamazaki") in view of Shimada and U.S. Published Application No. 2005/0023579 ("Yamazaki publication").

The claimed invention relates to a semiconductor integrated circuit device having a semiconductor element formed on a support substrate, the support substrate being a semiconductor substrate or a silicon on insulator (SOI) substrate. In one embodiment, inverter cells A' and B' may be used as standard cells of a standard cell type semiconductor integrated circuit device. In the inverter cells A' and B', source or drain regions 9 may be surrounded by element separation films 15 and gate electrodes 13 may be formed between the source regions or the drain regions 9. The inverter cells A' and B' may have one or more heat conduction parts connected to an input line, the gate electrodes and/or the source/drain regions. The head conduction parts may be formed of a plurality of via layers and metal wiring layers. The heat conduction parts may be formed such that the heat transmission paths are different from signal transmission paths. For more detail, please refer to the drawings, Figures 6-8, and to the specification, page 25, line 24+, although the claimed invention should not be limited to the preferred embodiments.

Yamazaki is directed to a semiconductor element having improved thin film transistor characteristics. The Office Action issued September 21, 2005 cites the "black mask 609" shown by Yamazaki in FIG. 9 as being a heat conduction part. However, the black mask 609 is produced by forming and patterning a metallic film (column 14, lines 59-62). This manufacturing process results in a black mask 609 made up of a metallic film formed as one solid layer and conforming to the shape of the second interlayer insulating film 607 (Fig. 9, No. 607; column 11, line 25). Therefore, because the black mask 609 is a metallic film formed as one solid layer, it is necessarily made up of only one layer of metal and cannot be construed to "include a plurality of metal wiring layers spaced apart from each other and arranged in a vertical stack" as recited by claim 18. Furthermore, because the black mask 609 is one layer of metal, it does not include "a plurality of metal via layers

connected to the metal wiring layers and coupling the metal wiring layers with each other" as is recited by claim 18.

Shimada is directed to wiring boards that have a plurality of wiring layers. The wiring board has a line 1, a shield pattern 2 disposed parallel with line 1 , conductive layers 4, 6, and conductive pillars 7a, 7b that connect the conductive layers 4, 6 (Shimada, FIG. 1). A line 11L and 13L formed on different wiring layers are connected by conductive pillars 7L and shielded by conductive layers 10S, 14S (Shimada, FIG. 3). Neither Yamazaki nor Shimada discloses or suggests a heat conduction part directly connected to an element separation film.

Yamazaki publication does not cure the deficiencies of the Yamazaki and Shimada combination. The Office Action relies on Figures 7-10 of the Yamazaki publication as disclosing inverter circuits having multilevel heat conduction parts which contact various portions of the inverter cells. (Office Action, p.3) Yamazaki publication is directed to a method of fabricating a semiconductor device using a crystalline semiconductor film formed by crystallizing an amorphous semiconductor thin film. Figures 7-10 disclose a sectional structure of a CMOS circuit having thin film transistors (TFTs) and method of fabricating the TFTs. It does not disclose a heat conduction part having "a plurality of metal via layers connected to the metal wiring layers and coupling the metal wiring layers with each other" as is recited by claim 18. For at least these reasons, Applicant respectfully submits that claim 18 should be allowable.

Claims 20-21, as renumbered, depend from claim 18 and therefore, should be likewise allowable.

Newly added claims 22-23 depend from claim 18. For at least the reasons mentioned above, claims 22-23 should be allowable.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
Ranga Sourirajan
Registration No.: 60,109
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant